

Call for Participation





IEEE Asian Solid-State Circuits Conference, A-SSCC 2018

Location: Shangri-La's Far Eastern Plaza Hotel (Tainan) Date: November 5 - November 7, 2018



Sponsored by IEEE SSCS, IEEE Region-10 SSCS Chapters

Conference Theme: Silicon Enabling Mobile Intelligence

The miniaturized silicon technology enabled big success in the realization of software solutions such as machine learning, big data, virtual and augmented realty in the image and speech recognition, the medical diagnosis and the autonomous driving automobiles. The current software solutions, however, consume huge power by employing cloud computers along with many graphic processing units and a large amount of memory. Nowadays, the integrated circuit design community tries to develop efficient low-power mobile intelligence solutions by taking challenges in the design of digital and analog circuits, processor architecture, and system for compact IoT devices.

The IEEE A-SSCC 2018 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia.

Conference Program

The conference technical program includes 4 plenary talks, 1 panel discussion, 1 industry session, and 4 tutorials. The 86 regular papers are grouped in 16 sessions covering analog circuits, data converters, digital circuits and systems, emerging technology and applications, memory, radio-frequency circuits, system-on-chip and signal processing, wireline and mixed signal circuits. The Student Design Contest will feature demos from the best student papers.

Plenary Talks



Dr. Kevin Zhang VP, Business Development, TSMC, Taiwan

"Circuit Design in Nano-Scale CMOS Technologies"

Dr. Nam Sung Kim SVP, Memory Division, Samsung, Korea

"Practical Challenges in Supporting Functions in Memory"

Panel Discussion "The Circuits and Systems for Mobile AI"

<u>Moderator</u>: Marvin, National Tsinghua Univ., Taiwan <u>Panelists / Position</u>:

- 1. AI Trends Overview: Marvin (National TH Univ)
- 2. Digital will win: Robert Chang (NCH Univ)
- 3. Analog is the MUST: JY Sim (Postech)
- 4. Low power schemes for AI: Kushida-San (Toshiba)
- 5. AI and Memory: Takeuchi-San (Chuyo Univ)
- 6. FPGA vs ASIC: Shouyi Yin (Tsinghua Univ)
- 7. Software vs Hardware: Leibo Liu (Tsinghua Univ)

Tutorials

- 1. Nan Sun (University of Texas at Austin): When SAR Meets ΔΣ A Tale of Two ADC Architectures -
- 2. Shuenn-Yuh Lee (NCKU): Wireless ECG Acquisition and Cardiac Stimulation SOCs for Body Sensor Networks
- 3. Minoru Fujishima (Hiroshima University): Terahertz CMOS Technology for Beyond 5G
- 4. Kyomin Sohn (Samsung Electronics): Memory System for Next Generation AI



Mr. Seizo ONOE CTA, NTT DOCOMO & President, DOCOMO Tech., Japan

"Open the New World of 5G"

Dr. Yi Kang Chief Scientist & SVP, UNISOC, China (Tsinghua Unigroup)

"AI Drive Domain Specific Processor"

Program at a Glance

DAY 1: Nov. 5 (Monday)			
08:30-18:00	Registration (B2F)		
09:00-10:30 (90)	Tutorial 1 (B1F)		
10:30-10:50 (20)	Break		
10:50-12:20 (90)	Tutorial 2 (B1F)		
12:20-13:40 (80)	Break		
13:40-15:10 (90)	Tutorial 3 (B1F)		
15:10-15:30 (20)	Break		
15:30-17:00 (90)	Tutorial 4 (B1F)		
17:00-19:00 (120)	SDC Exhibition (B1F)	FPGA Demo (B1F)	
18:00-19:30 (90)	Welcome Reception (B2F)		

DAY 2: Nov. 6 (Tuesday)						
07:45-18:00		Registration (B2F)				
08:30-08:50 (20)		Opening Ceremony (B2F)				
08:50-09:35 (45)		P1 : Plenary Talk 1 (B2F)				
09:40-10:25 (45)	P1 : Plenary Talk 2 (B2F)					
10:25-10:50 (25)	Break					
10:50-12:30 (100)] Advanced Techniqu	Industry 2 es for Industrial Applications	ET. Intelligent Sensor a	A 3 and Imager Systems	18	
12:30-13:30 (60)	Lunch			SDC	FPGA	
13:30-15:10 (100)	ACS 4 Power Converters and Sensors	FPGA 5 FPGA-based AI Computing	WLN 6 Optical Link and CDR	RF 7 Millimeter-Wave Transceivers and Terahertz Sensors	Exhibition (B1F)	Demo (B1F)
15:10-16:00 (50)	Break					
16:00-18:00 (120)	PD 8 : Panel Discussion (B2F)					
19:00-21:00 (120)	Banquet (B2F)					

DAY 3: Nov. 7 (Wednesday)				
07:45-12:00	Registration (B2F)			
08:30-09:15 (45)	P 9 : Plenary Talk 3 (B2F)			
09:20-10:05 (45)	P 9 : Plenary Talk 4 (B2F)			
10:05-10:30 (25)	Break			
10:30-12:35 (125)	ACS+DC 10 Analog and Data Converter Techniques	ETA 11 Technology and Circuit Techniques for IoT	MEM 12 Intelligent Memory System	DCS 13 Circuit Technologies for Security Enhancement
12:35-13:40 (65)	Lunch			
13:40-15:20 (100)	ACS 14 Inductive DC-DC Converters	DCS 15 Energy-Efficient Circuits and Architectures	WLN 16 Advanced Wireline Equalization	RF 17 Oscillators and Synthesizers
15:20-15:50 (30)	Break			
15:50-17:55 (125)	DC 18 (125) ADCs and Calibration Techniques	DCS+FPGA 19 (100) Multimedia and Signal Processing Hardware	SOC 20 (100) Intelligent Low-Power SoCs	RF 21 (100) Low-Power RF Transmitters and Receivers
17:55-19:30	Farewell Social Hour			

Registration Fees

	Early Bird		Regular Registration		
Category	Author	Non-Author		On-Site Registration	
3 5	Must register by	On & Before	On & After Oct. 1, 2018	jj	
	Sept. 9, 2018	Sept. 30, 2018			
Regular – IEEE Member	NT\$18000 (US\$600)		NT\$21000 (US\$700)	NT\$22500 (US\$750)	
Regular – IEEE SSCS Member	NT\$16500 (US\$550)		NT\$19500 (US\$650)	NT\$21000 (US\$700)	
Regular – Non Member	NT\$22500 (US\$750)		NT\$25500 (US\$850)	NT\$27000 (US\$900)	
Student – IEEE Member	—	NT\$9000 (US\$300)	NT\$12000 (US\$400)	NT\$13500 (US\$450)	
Student – IEEE SSCS Member	—	NT\$8250 (US\$275)	NT\$11250 (US\$375)	NT\$12750 (US\$425)	
Student – Non Member	—	NT\$10500 (US\$350)	NT\$13500 (US\$450)	NT\$15000 (US\$500)	
IEEE Life Fellow		NT\$9000 (US\$300)	NT\$12000 (US\$400)	NT\$13500 (US\$450)	

Tutorial Registration Fees (Free for all student attendees)

Category	1 Session	2 Sessions	Full Day (4 Sessions)	
Regular	NT\$2700 (US\$90)	NT\$4500 (US\$150)	NT\$6900 (US\$230)	
Student	Free	Free	Free	